ERI ELECTRONICS RESURGENCE INITIATIVE

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OPENROAD:

FOUNDATIONS AND REALIZATION OF OPEN, ACCESSIBLE DESIGN

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UC SAN DIEGO

THE CRISIS OF HARDWARE DESIGN …

- **ASIC design in advanced technologies: Huge barriers of Cost, Expertise and Risk**

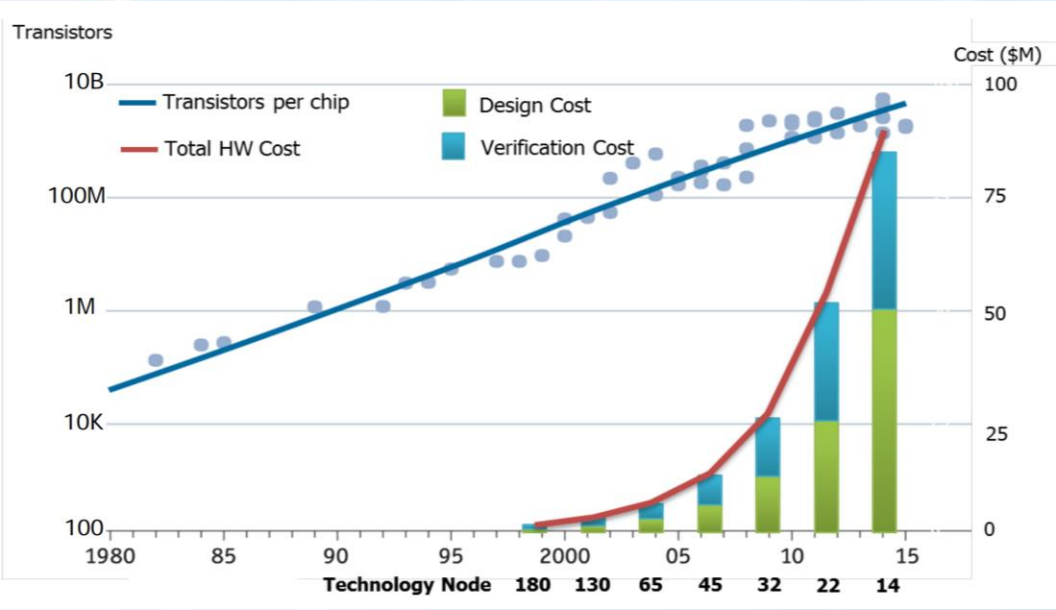


Image credit: A. Olofsson, keynote address, Intl. Symp. on Physical Design, March 2018

… IS A CRISIS OF INNOVATION

- Hardware innovators actually write code !
  - VHDL or Verilog that gets compiled into ICs

- The Real Crisis: Innovators are unable to evaluate their code in terms of SWaP and performance metrics

- Root Cause: The Crisis of Hardware Design

HOW IS ASIC DESIGN DONE TODAY?

- Very sophisticated tools with 1000's of commands
- Tool supplier focus: performance, power, area
- Large teams of expert users, many manual steps
- Long project schedules
- Significant project risks

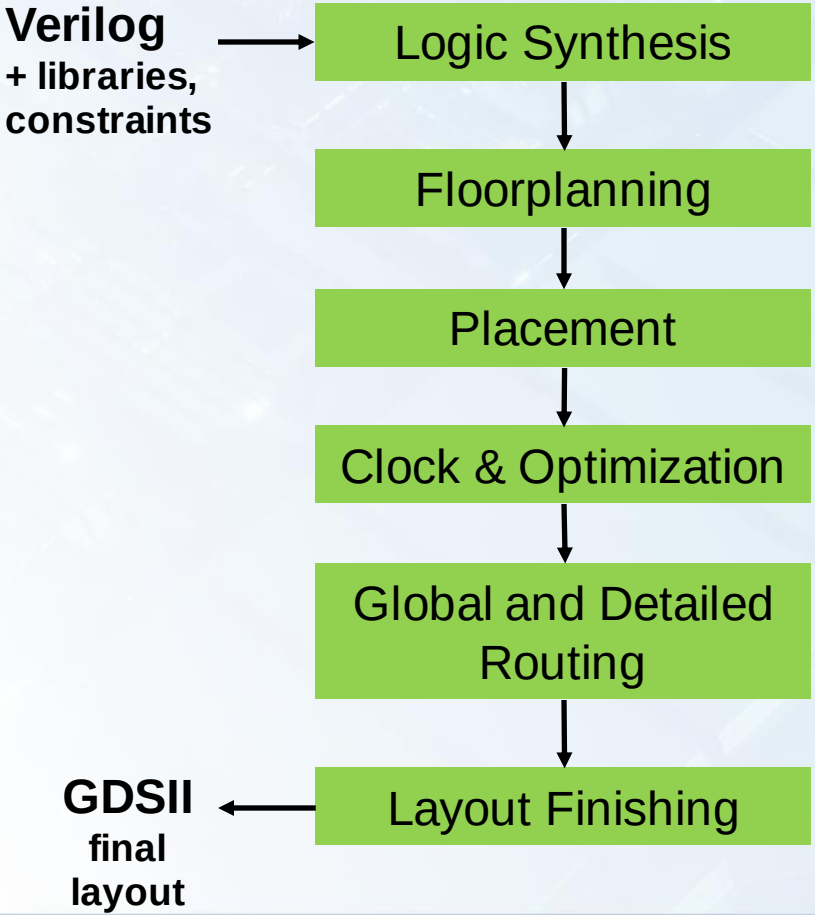
OPENROAD: NO HUMANS, 24 HOURS

- FOCUS: Ease of use and runtime

- Directly attack the crises of design and innovation
  - Schedule barrier: RTL-to-GDS in 24 hours
  - Expertise barrier: No-human-in-the-loop, tapeout GDS
  - Cost barrier: Open source (and runs in 24 hours)

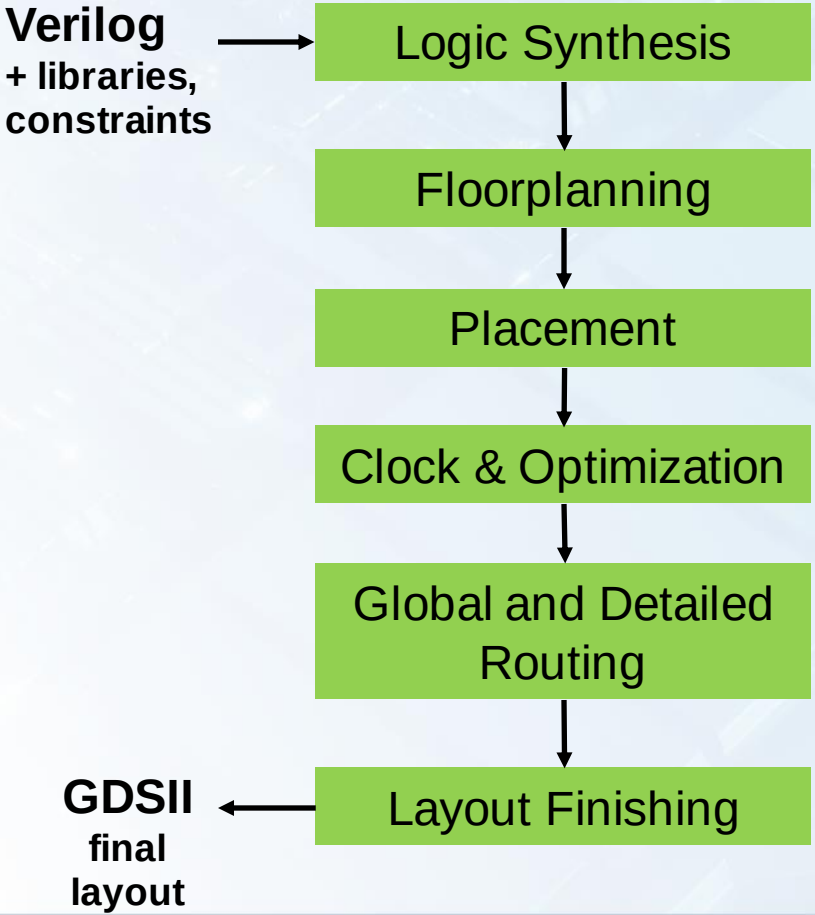
- Unleash system innovation and design innovation
- Enable tool customization to system, application needs

OPENROAD V2.0: WHAT'S NEW



- **Features**
  - **Early SOC planner**
  - **Parasitic extraction and timing signoff**
- **Usability**
  - **Tool qualification on new technology**
  - **Messages and documentation**
  - **Enhanced GUI**
- **Power-Performance-Area (PPA)**
  - **Logic synthesis, placement, clock tree, timing optimization**
  - **30% faster, 20% denser than v1.0**
    = a technology node of improvement
- **True no-human-in-the-loop: *Autotuner***

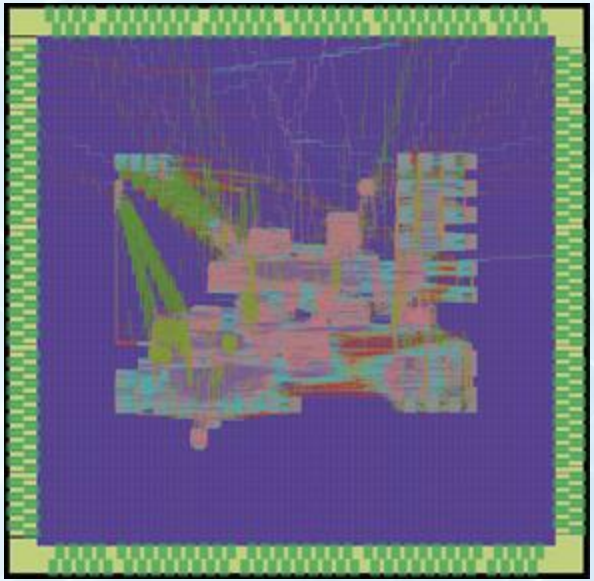
OPENROAD V2.0: REAL USAGE



- **SKY130: 100+ tapeouts on Google-SkyWater, Efabless chipIgnite shuttle**
- **GF12: Mixed-signal SOC tapeout**
- **Intel22: Army Research Labs project in flight**
- **Now supporting: GF12, Intel22, GF55, TSMC65, SKY90, SKY130 and more**

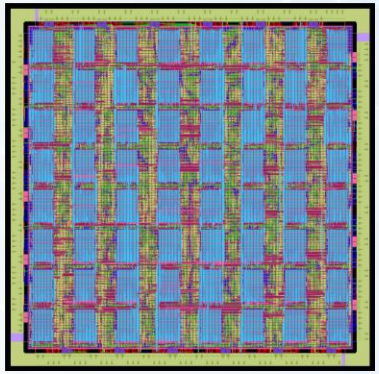
12NM SOC TAPE-IN: BLACKPARROT

- U. Washington RISC-V SoC
  - 1 CPU core, 360K cells, 53 macros
  - 3mm x 3mm package
- GLOBALFOUNDRIES 12LP
  - Invecas IOs
  - Arm standard cells / RAMs
- Output GDS DRC/LVS clean
  - Mentor Calibre verified
- RTL to GDS: < 5 hours

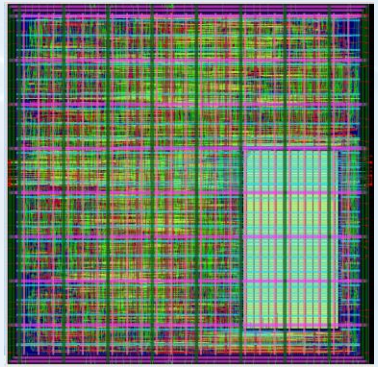


	target CP (ps)	WNS (ps)	TNS (ps)	fmax (MHz)	max skew (ps)	total WL (um)	#Insts	total power (W)
'golden' Oct20	8000	-894	-438729	112	813	9908654	795111	0.376
Current	6000	-580	-248060	152	583	8670446	730001	0.367
Improvement:	43%			36%	28%	12%	8%	2%

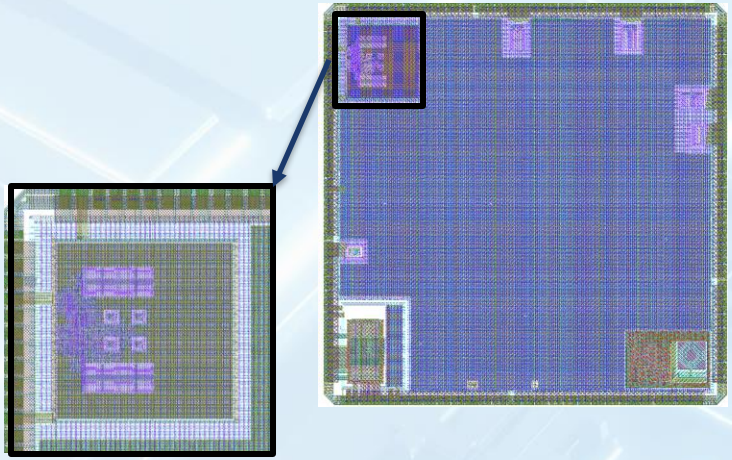
CREATED BY OPENROAD USERS



GF55 AI platform



GF12LP AI tile



OpenTitan SoC

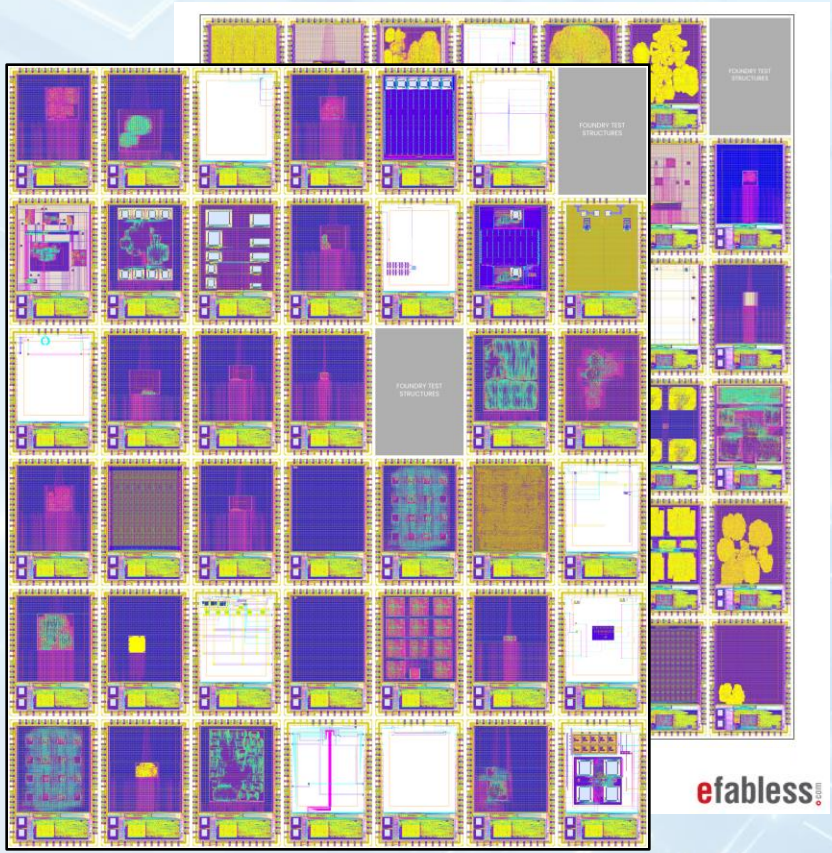
Army Research Labs
GF55, GF12LP

U. Michigan / FASoC
GF12LP

SKYWATER TECHNOLOGY 130NM

- 100+ tapeouts in SKY130
- Google-funded shuttle

- Efabless “chipIgnite” commercial offering
  - OpenROAD = default EDA flow



A GROWING USER COMMUNITY

- Users range from novice to expert
- Applications include Trust, 3DIC, AI/ML

- Community metrics all growing
  - 2-week period
  - Git clones (downloads), visitors, views

OPENROAD AVAILABILITY

- The Project on GitHub
  - https://github.com/The-OpenROAD-Project
- The Flow, developed by internal design advisors subteam
  - Automated full flow, built using tool components that are created for automation
  - https://github.com/The-OpenROAD-Project/OpenROAD-flow-scripts
- The Top-level Application
  - An integrated EDA tool focused on full automation
  - https://github.com/The-OpenROAD-Project/OpenROAD

NEXT: OPENROAD IN ACTION

- Design insight
- Timing debug
- Algorithm design and visualization
- Delivery of manufacturable layout

Architecture, integration and UI of a full-fledged EDA tool

OPENROAD IN ACTION

DESIGN INSIGHT

TIMING DEBUG

ALGORITHM DESIGN AND VISUALIZATION

MANUFACTURABLE LAYOUT

MANY BREAKTHROUGHS

- 12nm tapeout-proven tool from an academic research effort
- Integrated architecture, database, timing engine
- OpenROAD v2.0
  - Improved performance, power-efficiency, area

    ~1 technology node improvement of frequency, density
  - Machine learning and autotuning

    No-humans, 24-hours, DRC clean – with better results
  - 100+ user tapeouts from 130nm down to 12nm
- Engaged contributors: IBM, Google, DOD …

A foundation for research, innovation, and transitions

TRANSITIONS AND SUSTAINABILITY

- Growing a sustainable business + research ecosystem
  - Businesses will productize, distribute, support
  - Research ecosystem will innovate – faster
  - Special application, system needs will be better served
- Growing the technology
  - Machine learning → intelligence and self-adaptation
  - Cloud deployment → scale-up of both efficiency and quality
- Growing the user and developer community
  - Looking for DOD, DIB to join and guide this effort

FACULTY, INDUSTRY, EDA VETERANS

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